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Sample Problems, Set 1

1. Minimal Two-Level Forms

Provide minimal sum-of-products and product-of-sums expressions for the following functions.

- (a) $f(a,b,c,d) = \bar{a}bc\bar{d} + \bar{a}bcd + abc\bar{d} + ab\bar{c}d + a\bar{b}c\bar{d} + \bar{a}\bar{b}\bar{c}\bar{d} + \bar{a}\bar{b}\bar{c}\bar{$
- (b) $g(a,b,c,d) = a\bar{b}cd + a\bar{b}\bar{c}d + a\bar{b}\bar{c}\bar{d} + ab\bar{c}\bar{d} + abc\bar{d} + \bar{a}bcd + \bar{a}\bar{b}\bar{c}d + \bar{a}\bar{b}\bar{c}d + \bar{a}\bar{b}\bar{c}\bar{d} + abc\bar{d}$
- (c) $z(a,b,c,d,e,f) = abcdef + abcde\bar{f} + abcd\bar{e}\bar{f} + abc\bar{d}\bar{e}\bar{f} + a\bar{b}\bar{c}\bar{d}\bar{e}\bar{f} + ab\bar{c}\bar{d}\bar{e}\bar{f} + ab\bar{c}\bar$

2. More Minimal Two-level Forms

Consider the example shown in Figure 1: a 7-segment display decoder. The inputs are four bits, x_0, x_1, x_2, x_3 , specifying a number in binary. The outputs are 7 bits, a, b, c, d, e, f, g, specifying which segments to light up in a display – such as that of a digital alarm clock – to form the image of the corresponding decimal number. Our goal is to design a circuit that implements the functions a, b, c, d, e, f, g (with 0 corresponding to "off" and 1 corresponding to "on").

Since the four bits x_0, x_1, x_2, x_3 specify numbers from 0 to 15, but the display is only for 0 through 9, we'll adopt the convention that for inputs corresponding to 10, 11, 12, 13, 14 and 15 all the segments should light up (i.e., a through g evaluate to 1 for these inputs).

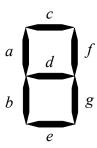


Figure 1: 7-Segment Display.

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Fill in the following to	ruth table.
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inputs							outputs				
x_3	x_2	x_1	x_0	a	b	c	d	e	f	g	
0	0	0	0								
0	0	0	1								
0	0	1	0								
0	0	1	1								
0	1	0	0								
0	1	0	1								
0	1	1	0								
0	1	1	1								
1	0	0	0								
1	0	0	1								
1	0	1	0								
1	0	1	1								
1	1	0	0								
1	1	0	1								
1	1	1	0								
1	1	1	1								

Find minimal sum-of-product and product-of-sums expressions for a,b,c,d,e,f and g.

3. Timing Analysis

For the circuits in Figures 2, 3 and 4, compute the arrival times for each output function for each input combination.

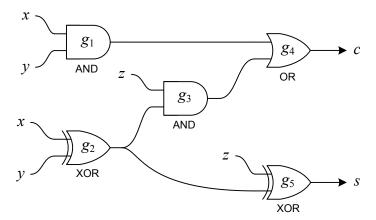


Figure 2: Circuit

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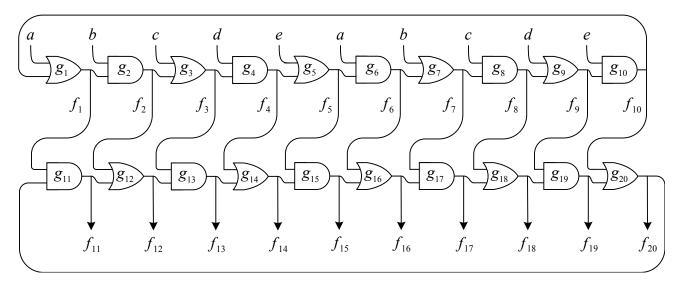


Figure 3: Circuit

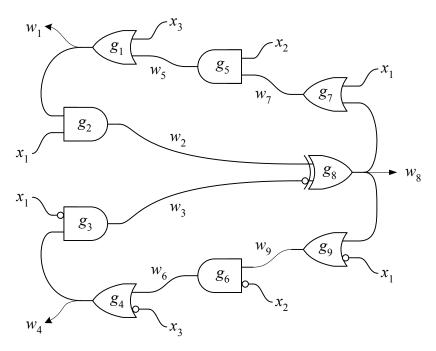


Figure 4: Circuit