# EXPERIMENT 4: COMBINATIONAL LOGIC DEVICES

### PURPOSE

In this experiment, we shall investigate some combinational logic devices, including full adders and decoders, plus seven-segment LED displays and drivers.

### INTRODUCTION

A wide variety of integrated circuits are available commercially, realizing many types of logical functions. These range from very simple functions found in devices such as sensors to extremely complex functions found in devices such as microprocessors. Some of the most complex integrated circuits have billions of transistors. (The current record, a chip by Altera, has 3.9 billion transistors). The feature sizes of these transistors range from micrometers, i.e., 10-6 meters, to nanometers, i.e., 10-9 meters. (Currently, the state of the art is 22 nanometers.)

Historically, integrated circuits were labeled MSI (for medium-scale integration), LSI (for large-scale integration) and VLSI (for very-large scale integration). The label VLSI is the most common one encountered these days.

In this experiment, we shall investigate two devices: the full adder and a decoder. While these are quite simple compared to devices like microprocessors, the functions that these devices implement are important. They are building blocks found in nearly all digital circuits.

### FULL ADDERS

Binary adders can be classified in a number of different ways. One classification is whether the device is a serial or parallel adder. Serial adders require the least amount of logic and are the slowest. They add each bit of the addend and augend to form the sum serially (sequentially one bit at a time with the time between bits determined by a clock signal). Parallel adders perform the additions of the bits of the addend and augend in parallel (all at the same time).

Another classification is whether it is a full or half adder. A half adder can sum only two bits, generating the sum and carry. On the other hand, a full adder forms the arithmetic sum and carry from three input bits. Two half-adders are needed to construct a full-adder. N full adders can be connected in tandem to realize an N-bit binary parallel adder, which can generate the sum of two N-bit binary numbers including the carry from the most significant bit.

### LED's and BCD-TO-SEVEN SEGMENT DECODER/DRIVERS

The 7447 BCD-to-seven segment decoder is used to drive a seven-segment LED display. The outputs, a-g, drive the corresponding segments on the seven-segment display according to the binary number present at the inputs A-D, D being the most significant bit of the number. Three additional inputs, LAMP TEST, BI/RBO, and RBI are provided. The blanking input/ripple-blanking output (BI/RBO) blanks (turns off) the display when set LOW. Otherwise, when BI/RBO is set high, the outputs drive the display according to the inputs A-D. The ripple blanking input (RBI) must be HIGH if blanking of a decimal zero is not desired. This input is useful in blanking higher order zeroes when using several displays for a multi-digit decimal number. Finally, LAMP TEST selects (turns on) all the segments when set LOW. It is used to test the segments on the display.

The display you will use is a TIL 321A common anode seven-segment LED display. This IC contains seven LED (light-emitting diode) segments. When forward biased, these diodes emit red light. Green and yellow LED's are also available. shows a schematic diagram of the display. In addition to the seven segment diodes, the display contains left and right decimal point diodes. In common anode displays, positive voltage (+5 V is sufficient) is applied to the either (or both) anode terminals. Whenever a 7447 segment driver output goes LOW, the segment diode to which it is connected becomes forward biased, and hence illuminated. With common cathode displays, ground is connected to the common cathodes, and the 7447 segment driver outputs go HIGH to forward bias the segment diodes. In either configuration, the current flow through the diodes must be limited. Forward biased diodes act as a short circuit. Without a restriction, the unconstrained current flow would burn out the diodes.



Figure 4.1 Schematic Diagram of TIL 321A LED Display.

The current required to illuminate the LED's is approximately 10 mA. The voltage drop across the diodes is approximately 1.7 V. Hence, (5.0 V - 1.7 V)/10 mA = 330 Ω resistors should be interposed between each 7447 output and its TIL 321A input, as illustrated in Figure 4.2.



Figure 4.2 Connection of 7447 to TIL 321A.

### PRELAB

1. Design and construct a 4-bit adder/subtracter using a 74LS283 4-bit binary adder and a 74LS86 Quad 2-input Exclusive-OR IC. The design should include four input lines for the addend/minuend, four input lines for the augend/subtrahend, and one control input line to select the operation--addition or subtraction. The inputs are 4-bit two’s complement numbers and the output sum is also a 2's complement number. Connect the inputs to the counter in the logic box, and connect output lines to a 7447 BCD-to-seven segment decoder/driver, which in turn is connected to a TIL 321A display. The carry out output from the adder can be connected to an LED on the logic box. The resistors you need to interpose between the TIL 321A and the 7447 are available in a DIP chip (4116R). The pin layout of the resistor chip is shown in . What is the longest propagation delay through only the 74LS283 binary adder? Assume a propagation delay of 9 nsec per gate.

Turn in the logic diagram and the chip layout diagram of the whole circuit (adder/subtracter, decoder/driver, resistors, 7-segment display).

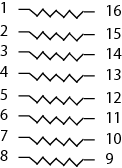


Figure 4.3 Pin layout of resistor array.

### PROCEDURE

Before performing the procedures listed below, read the report section of the experiment to assure you make all required measurements and record all required data.

When doing each step, include the results in the final report.

Test the adder/subtracter constructed in problem 1 of the Prelab on several additions and subtraction (including the ones specified by the Final Report). What "digit" on the display corresponds to each 4-bit input to the decoder/driver? Determine the maximum propagation delay *from any input of your circuit to the decoder/driver*. (Hint: you will need the logic diagram of 74LS283.) Demonstrate to your TA that your circuit works correctly when you complete the table in part 1-b in your final report.

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# FINAL REPORT

**I. *Binary Adder/Subtracter***

a). Sketch the logic diagram for your adder/subtracter circuit below:

b). Complete the following table of additions and subtractions performed by your circuit. Indicate whether or not the carry/borrow LED is on (1) or off (0) and the "digit" in the LED display. Are the results correct? Demonstrate to your TA that the table is completed based on your circuit behavior. Your TA must initialize the completed table.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Addend/Minuend | Augend/Subtrahend | carry SUM | | carry DIFFERENCE | |
| 0011 | 0101 |  |  |  |  |
| 0010 | 1110 |  |  |  |  |
| 1000 | 0111 |  |  |  |  |
| 1001 | 0101 |  |  |  |  |
| 0101 | 0110 |  |  |  |  |
| 1111 | 0110 |  |  |  |  |
| 0110 | 1111 |  |  |  |  |
| 0000 | 1000 |  |  |  |  |

c). Draw the "digit" on the LED display that corresponds to each 4-bit input to the 7447 BCD-to-seven segment decoder/driver.

d). Sketch the displays observed on the oscilloscope when trying to determine the maximum propagation delay *from any input of your circuit to the decoder/driver*. Indicate the longest path on your logic diagram shown in part 1 above.



**LOW to HIGH Output Transition**



**HIGH TO LOW Output Transition**

e). What is the maximum propagation delay?

**II. *Conclusion***

Comment on the advantage and disadvantage of this approach to constructing a subtracter using an adder as opposed to constructing a separate subtracter circuit.